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09/811,444	03/20/2001	Takashi Kobayashi	500.39879X00	9563

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EXAMINER	
QUINTO, KEVIN V	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/811,444	Applicant(s) KOBAYASHI, TAKASHI
	Examiner Kevin Quinto	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) *15-42* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 11-14* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Claims 15-42 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 8-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 8 recites the limitation "said second gate insulating film" in the third paragraph of the claim. There is insufficient antecedent basis for this limitation in the claim.

6. It is the examiner's belief that the "said second gate insulating film" is the same film described towards the end of the second paragraph of claim 8. To be more specific, the examiner believes that "a second insulating film" of the limitation "second gate electrodes formed on said

third well with the interposition of a second insulating film" is the same as "said second gate insulating film."

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 2, 4, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cappelletti et al. (USPN 6,410,387 B1) in view of Shum et al. (USPN 6,327,182 B1).

9. In reference to claim 1, Cappelletti et al. (USPN 6,410,387 B1, hereinafter referred to as the "Cappelletti" reference) discloses a similar device. Figure 20 discloses a nonvolatile semiconductor memory device. The memory cell region is in the middle of this figure and has a first MOS field effect transistor, a floating gate (7), and a control gate (29). It is understood that what is shown is one unit cell of a memory cell array comprising a plurality of memory cells arranged as a matrix. The memory cell region in the device of Cappelletti does not have its own dedicated well within the substrate. However a nonvolatile semiconductor device having a memory cell portion which uses its own dedicated well is well known in the art. Shum et al. (USPN 6,327,182 B1, hereinafter referred to as the "Shum" reference) discloses a nonvolatile semiconductor device in figure 9 which uses a memory cell portion that has its own well within the substrate. Shum further discloses (in column 5, lines 28-40) that a memory cell portion which is in a separate well "allows biasing during operation of the memory cells with a reduced

likelihood of disturbing non-selected memory cells." It would therefore be obvious to use a separate well for the memory cell portion in the device of Cappelletti in order to avoid disturbing non-selected memory cells. Thus in the device of Cappelletti constructed in view of Shum, there is a floating gate (7) and control gate (29) formed on a well. There is a first diffusion layer which function as a source (30) and a drain (31). There is a tunnel dielectric film (5) between the well and the floating gate (7). There is also an interpoly dielectric film (18) between the floating gate (7) and the control gate (29). Figure 20 of Cappelletti also shows a peripheral circuit region to the right of the memory cell region. Within the peripheral circuit region, there is a second MOS field effect transistor which has a second well (21) formed in the substrate (1). There is a second diffusion layer formed in the second well (21) which functions as a source (44) and a drain (45). There is a gate electrode (26) which is formed on the second well (21) with the interposition of a gate insulating film (24). This gate insulating film (24) is also the first insulating film which is deposited on the semiconductor substrate (1). It is also understood that there is a plurality of these second MOS field effect transistors. As can be seen in the figure, shallow groove or trench isolation is utilized for isolation of the second MOS field effect transistors.

10. In reference to claim 2, the first insulating film (24) of Cappelletti is understood to be silicon oxide (column 5, line 1).

11. With regard to claim 4, Cappelletti discloses that the interpoly dielectric film is made of three deposited layers (oxide-nitride-oxide, column 4, lines 24-25). The first such oxide meets the claim limitation, "a second deposited insulating film." Cappelletti and Shum teach all of the

claimed invention except for the exact thickness of the second deposited insulating film.

Although Cappelletti and Shum do not teach the exact thickness as that claimed by Applicant:

> The shape, size, dimension differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note In re Leshin, 125 USPQ 416.

Therefore claim 4 is not patentably distinguishable over the Cappelletti and Shum references.

12. In reference to claim 5, it is understood that the first oxide layer of the interpoly dielectric or the second insulating film (24) is silicon oxide.

13. In reference to claim 8, Cappelletti et al. discloses a similar device. Figure 20 discloses a nonvolatile semiconductor memory device. The memory cell region is in the middle of this figure and has a first MOS field effect transistor, a floating gate (7), and a control gate (29). It is understood that what is shown is one unit cell of a memory cell array comprising a plurality of memory cells arranged as a matrix. The memory cell region in the device of Cappelletti does not have its own dedicated well within the substrate. However a nonvolatile semiconductor device having a memory cell portion which uses its own dedicated well is well known in the art. Shum et al. (USPN 6,327,182 B1, hereinafter referred to as the "Shum" reference) discloses a nonvolatile semiconductor device in figure 9 which uses a memory cell portion that has its own well within the substrate. Shum further discloses (in column 5, lines 28-40) that a memory cell portion which is in a separate well "allows biasing during operation of the memory cells with a reduced likelihood of disturbing non-selected memory cells." It would therefore be obvious to use a separate well for the memory cell portion in the device of Cappelletti in order to avoid disturbing non-selected memory cells. Thus in the device of Cappelletti constructed in view of Shum, there is a floating gate (7) and control gate (29) formed on a well. There is a first diffusion layer which function as a source (30) and a drain (31). There is a tunnel dielectric film

(5) between the well and the floating gate (7). There is also an interpoly dielectric film (18) between the floating gate (7) and the control gate (29). Figure 20 of Cappelletti also shows a peripheral circuit region to the left and right of the memory cell region. Within the peripheral circuit region, there is a second MOS field effect transistor which has a second well (21) formed in the substrate (1). There is a second diffusion layer formed in the second well (21) which functions as a source (44) and a drain (45). There is a gate electrode (26) which is formed on the second well (21) with the interposition of a first gate insulating film (24). It is understood that there is a plurality of these second MOS field effect transistors. There is a third MOS field effect transistor which has a third well (15) formed in the substrate (1). There is a third diffusion layer formed in the third well (15) which functions as a source (16) and a drain (17). There is a second gate electrode (8) which is formed on the third well (21) with the interposition of a second gate insulating film (3). This second gate insulating film (3) is thicker than the first insulating film (24). As can be seen in the figure, shallow groove or trench isolation is utilized for isolation of the peripheral circuit region.

14. In reference to claim 9, the second gate insulating film (3) or first insulating film is understood to be silicon oxide.

15. In reference to claim 11, the applicant states that the "interpoly dielectric film and the first gate insulating film comprises a second deposited insulating film." The examiner believes that the applicant is stating that the silicon oxide film of the interpoly dielectric film and the silicon oxide film which makes up the first gate insulting film are formed in the same step (as seen in figure 2B of the specification). However this places claims 11, 12, and 13 into the form of a product-by-process claim:

> Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Thorpe, 227 USPQ 964, 966; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in " product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 2113.

Claims 11-13 do not distinguish over the Cappelletti and Shum references regardless of the process used to form the silicon oxide film of the interpoly dielectric and the first gate insulating film, because only the final product is relevant, and not the process of making such as forming the silicon oxide film of interpoly dielectric film and the silicon oxide film which makes up the first gate insulating film in the same step.

16. In reference to claim 12, the second insulating film or the first gate insulating film (24) and the first insulating film or the second gate insulating film (3) of Cappelletti are understood to be silicon oxide (column 3, lines 2-6 and column 5, lines 1-4).

17. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cappelletti et al. (USPN 6,410,387 B1) in view of Shum et al. (USPN 6,327,182 B1) and further in view of Nakanishi (JP 01033935 A).

18. In reference to claim 3, neither Cappelletti nor Shum discloses the use of nitrogen in the gate insulating film of the second MOS field effect transistor. However the use of nitrogen in a gate insulating film is well known in the art. Nakanishi (JP 01033935 A) discloses a gate insulating film which is annealed in a nitrogen atmosphere therein introducing a nitrogen concentration into the film. The addition of the nitrogen brings the benefits of fewer traps, a thinner film, high reliability, and excellent breakdown strength (abstract). It would therefore be obvious to use a gate insulating film with a nitrogen concentration in the device of Cappelletti constructed in view of Shum so as to gain these advantages.

19. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cappelletti et al. (USPN 6,410,387 B1) in view of Shum et al. (USPN 6,327,182 B1) and further in view of Nakanishi (JP 01033935 A).

20. In reference to claim 10, neither Cappelletti nor Shum discloses the use of nitrogen in the gate insulating film of the second MOS field effect transistor. However the use of nitrogen in a gate insulating film is well known in the art. Nakanishi (JP 01033935 A) discloses a gate insulating film which is annealed in a nitrogen atmosphere therein introducing a nitrogen concentration into the film. The addition of the nitrogen brings the benefits of fewer traps, a thinner film, high reliability, and excellent breakdown strength (abstract). It would therefore be obvious to utilize a second insulating film with a nitrogen concentration in the device of Cappelletti constructed in view of Shum so as to gain these advantages.

21. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cappelletti et al. (USPN 6,410,387 B1) in view of Shum et al. (USPN 6,327,182 B1) and further in view of Nakanishi (JP 01033935 A) and further in view of Gardner (USPN 6,259,133 B1).

22. In reference to claim 6, neither Cappelletti nor Shum discloses the use of nitrogen in the gate insulating film of the second MOS field effect transistors. However the use of nitrogen in a gate insulating film is well known in the art. Nakanishi (JP 01033935 A) discloses a gate insulating film which is annealed in a nitrogen atmosphere therein introducing a nitrogen concentration into the film. The addition of the nitrogen brings the benefits of fewer traps, a thinner film, high reliability, and excellent breakdown strength (abstract). It would therefore be obvious to utilize a first and a second gate insulating film with a nitrogen concentration in the device of Cappelletti constructed in view of Shum so as to gain these advantages. Neither of the

above-cited references discusses the use of an interpoly dielectric which has a nitrogen content. However the use of such an interpoly dielectric is well known in the art. Gardner et al. (USPN 6,259,133 B1, hereinafter referred to as the "Gardner" reference) discloses that an interpoly dielectric with a nitrogen content has an improved quality due to a decreased density of interface trap states (column 12, lines 42-45). It would therefore be obvious to use an interpoly dielectric film with a nitrogen content.

23. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cappelletti et al. (USPN 6,410,387 B1) in view of Shum et al. (USPN 6,327,182 B1) and further in view of Nakanishi (JP 01033935 A) and further in view of Gardner (USPN 6,259,133 B1).

24. In reference to claim 13, neither Cappelletti nor Shum discloses the use of nitrogen in the gate insulating film of the first and second MOS field effect transistors. However the use of nitrogen in a gate insulating film is well known in the art. Nakanishi (JP 01033935 A) discloses a gate insulating film which is annealed in a nitrogen atmosphere therein introducing a nitrogen concentration into the film. The addition of the nitrogen brings the benefits of fewer traps, a thinner film, high reliability, and excellent breakdown strength (abstract). It would therefore be obvious to utilize a first and a second gate insulating film with a nitrogen concentration in the device of Cappelletti constructed in view of Shum so as to gain these advantages. Neither of the above-cited references discuss the use of an interpoly dielectric which has a nitrogen content. However the use of such an interpoly dielectric is well known in the art. Gardner et al. (USPN 6,259,133 B1, hereinafter referred to as the "Gardner" reference) discloses that an interpoly dielectric with a nitrogen content has an improved quality due to a decreased density of interface

trap states (column 12, lines 42-45). It would therefore be obvious to use an interpoly dielectric film with a nitrogen content.

Allowable Subject Matter

25. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

26. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests a nonvolatile semiconductor memory device where the nitrogen content is higher in the memory cell interpoly dielectric than the peripheral circuitry gate dielectric.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (703) 306-5688. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

KVQ
July 29, 2002

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